Attorney Docket No. 42P15042

APPLICATION FOR UNITED STATES LETTERS PATENT

For

AN ENHANCED GATE STRUCTURE

Inventor(s):

John Barnak

Mark Doczy

Robert S. Chau

Reza Arghavani

Collin Borla

Prepared by:

BLAKELY SOKOLOFF TAYLOR & ZAFMAN LLP
12400 Wilshire Boulevard
Seventh Floor
Los Angeles, CA 90025-1026
(408) 720-8300

"Express Mail" mailing label number: EV336581243US
Date of Deposit: August 29, 2003
I hereby certify that I am causing this paper or fee to be deposited with the United States Postal Service "Express Mail Post Office to Addressee" service on the date indicated above and that this paper or fee has been addressed to the Assistant Commissioner for Patents, Washington, D. C. 20231

Christopher P. Marshall
(Typed or printed name of person mailing paper or fee)

C.P. Marshall
(Signature of person mailing paper or fee)

8/29/2003
(Date signed)

AN ENHANCED GATE STRUCTURE

FIELD

[0001] Embodiments of the invention relate to semiconductor manufacturing. More particularly, embodiments of the invention relate to the formation of a silicon-nitride layer between a polysilicon gate structure and a dielectric within a complementary metal-oxide-semiconductor (CMOS) device.

BACKGROUND

[0002] Typical CMOS devices have gate structures consisting of a dielectric layer deposited upon the device substrate and a polysilicon or metal gate structure deposited upon the dielectric layer. Figure 1 illustrates a typical CMOS device having a prior art gate structure. Gate structures, such as those in Figure 1, however, may experience adverse electrical effects or defects over time, including short circuits forming between the transistor gate material and the dielectric, pinning of the transistor gate material work function, and excessive defect densities between the transistor gate material and the dielectric. Pinning can occur when a defect within the polysilicon/gate oxide interface, and the work function of the gate electrode becomes approximately equal to the energy level or ban of energy levels of the defect.

[0003] Some of these adverse effects or defects may arise from adhesion problems between the dielectric layer and transistor gate material, such as doped polysilicon. Adhesion problems may arise due to high-temperature exposure of the gate structure during processing or cycling the gate voltage over time. As a result, the performance as well as the reliability of the transistor can be reduced.

BRIEF DESCRIPTION OF THE DRAWINGS

[0004] Embodiments of the invention are illustrated by way of example and not limitation in the figures of the accompanying drawings, in which like references indicate similar elements and in which:

[0005] Figure 1 is a typical transistor containing a prior art gate structure.

[0006] Figure 2 is a CMOS device containing gate structures according to one embodiment of the invention.

[0007] Figure 3 is a flow diagram illustrating a portion of a semiconductor process that may be used in conjunction with one embodiment of the invention.

DETAILED DESCRIPTION

[0008] Embodiments of the invention described herein relate to complementary metal-oxide-semiconductor (CMOS) processing. More particularly, embodiments of the invention relate to the creation of a gate structure in a transistor that is substantially resistant to defects, such as short circuits forming between the transistor gate material and the dielectric, pinning of the transistor gate material work function, and excessive defect densities between the transistor gate material and the dielectric.

[0009] Figure 2 illustrates a CMOS device in which one embodiment of the invention may be used. The device of Figure 2 is an inverter, which comprises an n-type transistor 205 and a p-type transistor 210. In each of the transistors is a dielectric layer 215, a polysilicon gate 218, and a buffer 217, across which an electric field is created when a gate voltage is applied to the gate 225 while the body 220 is biased at a lower potential than the gate. In the n-type transistor, the polysilicon gate is doped with n-type material, whereas in the p-type transistor, the polysilicon gate is doped with p-type material.

[0010] The buffer is a layer that may be formed upon the dielectric through various processing techniques, including physical vapor deposition (PVD). In one embodiment of the invention, the buffer contains silicon doped with nitrogen to form a silicon nitride layer between the polysilicon gate and the dielectric layer.

[0011] Advantageously, the silicon-nitride buffer reduces defect densities between the transistor polysilicon gate material and the dielectric layer. Furthermore, the buffer helps prevent electrical shorts from forming between the

dielectric and the polysilicon gate while reducing pinning of the gate work function.

[0012] In the embodiment illustrated in Figure 2, the dielectric layer has a substantially high dielectric constant in order to allow the dielectric layer to be as thin as possible while still being able to support the electric field produced by the voltage applied to the gate. For example, the dielectric layer of Figure 2 has dielectric constant greater than twenty.

[0013] Figure 3 is a flow diagram illustrating a number of operations in a semiconductor manufacturing process according to one embodiment. At operation 301, a substrate is formed within a silicon wafer. A source and drain are formed within the substrate at operation 305. A dielectric layer is formed upon the substrate at operation 310, and the silicon-nitride buffer is formed upon the dielectric layer using a physical vapor deposition (PVD) process at operation 315. Polysilicon gate material is then applied upon the silicon-nitride buffer at operation 320.

[0014] While the invention has been described with reference to illustrative embodiments, this description is not intended to be construed in a limiting sense. Various modifications of the illustrative embodiments, as well as other embodiments, which are apparent to persons skilled in the art to which the invention pertains are deemed to lie within the spirit and scope of the invention.